REMARKS

In an Office Action mailed July 15, 2004, pending claims 1-15 were examined and rejected. In response, Applicant is submitting distinguishing remarks and respectfully request the reconsideration and allowance of claims 1-15, thereby placing the application in condition for allowance. No additional fees are required as a result of this communication.

Claims 1-3, 5-7, 9-11, 13 and 14 were rejected under 35 U.S.C. 103(a) as being obvious over Blomgren et al. (U.S. Patent 6,275,838) in view of Zou et al. (U.S. Patent 6,425,070). In the stated rejection, Applicant was directed to Figure 8B of Blomgren and to Figure 8 of Zou. The floating point pipeline of Figure 8B of Blomgren is a continuation of the floating point pipeline of Figure 8A. Blomgren states at Col. 11, lines 26-33 that the multiplier 832 produces a redundant sum. A redundant sum is two partial sums of partial product values which when added result in the product. Blomgren does not teach, as recited in claim 1, "a multiplier array ...providing a sum and a carry." Blomgren does not teach or suggest the use of a carry value in the floating point pipeline of Figure 8A or 8B. Additionally, Blomgren does not teach or suggest a floating point multiplier and accumulator as recited in claim 1 having "multiplexor circuitry coupled to the multiplier array for selectively bit shifting each of the sum and the carry" as recited as having been provided by the multiplier.

Zou was cited for the proposition of teaching in Figure 8 "a multiplexor circuitry coupled to the multiplier array for selectively bit shifting each of the sum and carry." The only multiplexor taught by Zou in Figure 8 is mux 901 which is not functionally related to or coupled in a functional manner to multiplier 902. Additionally mux 901 does not selectively bit shift any value. As described at Col. 16, lines 4-9, mux 901 selects between one of two output values and directly outputs the selected value. As stated at Col. 16, lines 41-47, the shifting that is performed by the Zou multiplier accumulator unit is performed during the same clock cycle as either the multiply or the accumulate operation to reduce clock cycles to perform double precision. Further, mux 901 of Zou does not process either a sum or a carry value from a multiplier in contrast to the multiplexor circuitry recital of claim 1. It should be noted that multiplier 902 of Zou is represented as providing a single output value, the product of two 17-bit

values. Therefore, the combination of the multiplier unit of Zou with the floating point pipeline of Blomgren does not teach or suggest the recited structure and functionality of rejected claim 1.

Claim 2 was rejected on the basis of Blomgren disclosing adder circuitry having a first input for receiving a sum and a second input for receiving a carry. As stated above, Blomgren clearly state that the multiplier 832 provides a redundant sum (Col. 11, line 29) and does not teach or suggest the bifurcation of sum and carry outputs. While Blomgren teach the use of feedback to the multiplier input prior to a normalizer and a rounder function, the previously discussed recitals of claim 1 make claim 3 also allowable.

Claim 5 was rejected on the basis of Blomgren in which multiplexors 800a through 800c were stated to be registers. The Blomgren floating point unit teaches a single register file 840 for storing operands. The operands selected by multiplexors 800a through 800c are not taught as being stored by the multiplexors. As taught by Applicant in the specification, the presence of the recited registers of claim 5 is optional in the claimed subject matter. However, when present, the location of the registers and multiplexors in the claimed structure is different than the structure of the Blomgren floating point unit.

Claim 6 was rejected by noting that Blomgren does not disclose the recited control circuitry and functionality of claim 6. Instead, Figure 8 of Zou was used as the basis for obviousness. Neither Blomgren nor Zou teach or suggest a multiplexor that is controlled to bit shift a sum and a carry generated by a multiplier array as recited in claim 6. While control signals for shifters and multiplexors are well known in the art, the recited structure of claim 6 noted herein is not taught by either reference.

Claim 7 was rejected on the basis of Blomgren teaching a floating point exponent logic 870 to predict the result's exponent. However, Blomgren does not teach at Col. 11, lines 8-10 how the prediction is implemented.

Claims 9 and 10 were rejected by noting that Blomgren does not disclose the recited bit shifting but that Zou discloses a right shifter 900 in Figure 8. As stated above, neither Blomgren nor Zou teach or suggest the use of a multiplexor that bit shifts a sum and a carry. Therefore, claim 10 is readily distinguishable over Blomgren and Zou. While shifting functions are common in semiconductors, neither Blomgren nor Zou teach the recited shifting circuitry of claim 9 for shifting the recited third operand or the resultant operand.

Claim 11, an independent claim, was rejected under the same rationale as provided for claim 1. However, claim 11 is a method claim and is of different scope than the previously rejected claims. In addition to the differences noted above, other recited differences exist. Neither Blomgren nor Zou teach "selectively bit shifting the sum and the carry based upon: (1) a number of leading zero bits of a resultant operand of a previous calculation; (2) exponent values of the first operand and the second operand; and (3) an exponent value of the resultant operand of the previous calculation" as recited in claim 11.

Claim 13 was rejected on the same basis as claim 7. However, as noted above, Blomgren does not teach how the prediction is implemented.

Claim 14 was rejected under the same rationale as claim 1. However, claim 14 is a method claim and is of different scope than rejected claim 1. In addition to the differences noted above, other recited differences exist. Neither Blomgren nor Zou teach "selectively bit shifting each of the sum and the carry and selectively adding a plurality of logic zero bits into a portion of the sum and carry in response to control signals created using exponential values of the first operand, the second operand and the third operand and a previous resultant exponential value" as recited in claim 14.

Therefore, Applicant respectfully requests the reconsideration of and the withdrawal of the rejection of claims 1-3, 5-7, 9-11, 13 and 14 under 35 U.S.C. 103(a).

Claims 4, 8, 12 and 15 were rejected under 35 U.S.C. 103(a) as being obvious over Blomgren et al. (U.S. Patent 6,275,838) in view of Zou et al. (U.S. Patent 6,425,070) as applied to claim 1 above, and further in view of Montoye et al. (U.S. Patent 4,969,118). Applicant submits that dependent claims 4, 8, 12 and 15 are allowable over this combination for the same reasons stated above as Montoye et al. do not teach or suggest the missing elements and functions noted above. Montoye teach a floating point unit with a multiplier 12 that according to Col. 4, lines 44-47, provides two addends whose sum is mantissa A multiplied by mantissa B. Thus, Montoye also does not use a multiplier analogous to the multiplier recited in the rejected base claims that provides a sum and a carry. Montoye was cited for the proposition of teaching the recited selective inverter or selective inverting function of claims 4, 8, 12 and 15. Blomgren and Zou were acknowledged as not disclosing this function or circuitry. The Montoye circuitry that was stated to be analogous circuitry was identified as complementer 22 of FIG. 1.

Regarding claim 4, Montoye also does not teach "selective inversion occurring prior to feeding the mantissa portion of the resultant operand back to the multiplier array" as recited in claim 4. In the rejection basis of claim 8, element 20, an incrementer, was stated to be a "selective inverter 20." As described at Col. 5, lines 12-20, incrementer 20 does no bit inversion but rather increases or increment the overflow of shifter 14. Regarding claim 8, Montoye does not teach "a selective inverter coupled to the register" nor a selective inverter "having an output coupled to the shifting circuitry." Regarding claim 12, Montoye does not teach "selectively using the cumulative sum in a subsequent multiply/accumulate operation, in inverted or non-inverted form, as one of the first operand or the second operand when the cumulative sum is not subsequently used as the third operand, the cumulative sum not being normalized or rounded prior to such use as one of the first operand or the second operand." Regarding claim 15, Montoye does not teach "inverting logic state of all bits of the resultant operand prior to using the resultant operand as one of the first operand, the second operand or the third operand in a subsequent calculation." Therefore, Applicant respectfully requests the reconsideration and withdrawal of the stated rejection of claims 4, 8, 12 and 15.

The teachings of Kobunaya (U.S. Patent 5,185,713), Andreas (U.S. Patent 5,517,436) and Kowalczyk (U.S. Patent 5,450,607) that were not relied upon as a rejection basis were stated to be pertintent to the present disclosure. However, each patent discloses a multiplier structure and operation that is readily distinguishable from the recited structures and methods of claims 1-15.

Applicant respectfully requests consideration of the amendments and the allowance of claims 1-15, thereby placing the application in condition for allowance. Should issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned at (512) 996-6839.

Respectfully submitted,

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